Effective Charge Density (N_{eff}) in MOS Structures Fabricated on High Index Silicon Wafers.

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Summary

The MOS technology was originally developed on the (0 0 1)-Si surface because this orientation presents the lowest charge density at the interface, thus leading to higher device performance than that from other orientations [1,2]. Nevertheless, under certain thermal conditions, it is possible to obtain lower charge densities using high index Si wafers [3]. (1 1 4) and (5 5 12)-Si presents a periodical surface roughness that may have some potential applications in CMOS technology [4]; therefore, it is important to investigate the charge density in MOS structures fabricated on these Si orientations.

Experimental

Using the (0 0 1), (1 1 1) and (1 1 0)-Si orientations as references, we characterized the MOS effective charge in (1 1 4) and (5 5 12)-Si for 4 fabrication processes. Table I shows the experimental matrix.

Table I. Orientation, gate material, type, and number of wafers used in the fabrication processes (**A**-**D**).

	(0 0 1)	(1 1 4)	(5 5 12)	(1 1 1)	(1 1 0)	Gate
A	2, n	2, n	4, n	-	-	Poly
B	2, n	2, n	2,n. 2,p	-	-	Poly
C	1, n	1, n	1, n	1, n	1, p	Al
D	1, n	1, n	1, n	1, n	1, p	Al

A was a standard CMOS process, **B** was a p-well MOS-process, whereas **C** and **D** were just MOS capacitor processes. We designed the process in order to obtain a gate oxide thickness in (0 0 1) of ~600Å for **A**, **B** and **C;** the thickness was ~150Å for **D** process.

Results

The effective charge density was obtained using the flat band shift in C-V measurements for all the processes; the results are shown in Figs. 1-4. The **A** CMOS process shows that there is not an appreciable dependence of N_{eff} on the type and doping density of the substrate, Fig. 1. In the **A** CMOS process we observed that N_{eff} increases for the high index orientations, whereas the (1 1 4) orientation from the **B** p-well process presents a N_{eff} close to that of the (0 0 1)-Si, Fig. 2.

According to Figs. 3 and 4, in **C** and **D** processes a negative effective charge (Q_{eff}<0) was obtained for some samples, including the (0 0 1) orientation. The minimum value for N_{eff}, was obtained even for non (0 0 1)-Si orientations. The origin and ordering of these values will be discussed at the time of the conference.

Acknowledgments

This work was supported by CONACyT-Mexico under grant 39886 and scholarship 158493.

References

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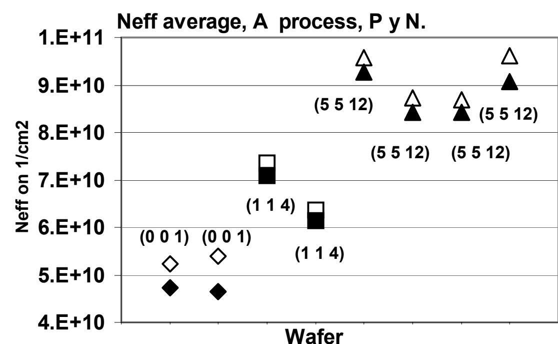

Figure 1. Effective charge density in **A** process. Filled symbols for p-MOS, and empty for n-MOS capacitors.

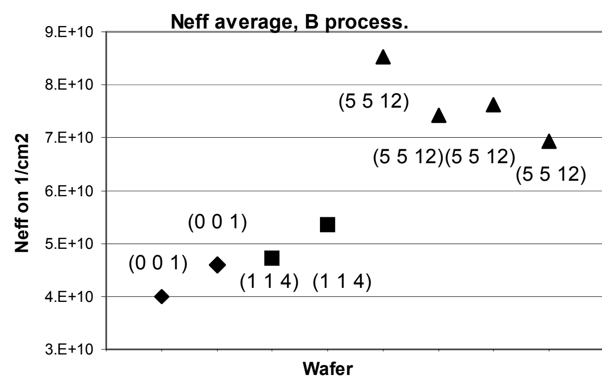

Figure 2. Effective charge density obtained in **B** process.

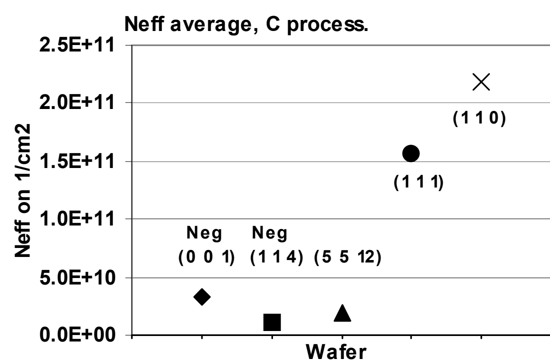

Figure 3. Effective charge density obtained in **C** process. The label **Neg** indicates a negative Q_{eff}.

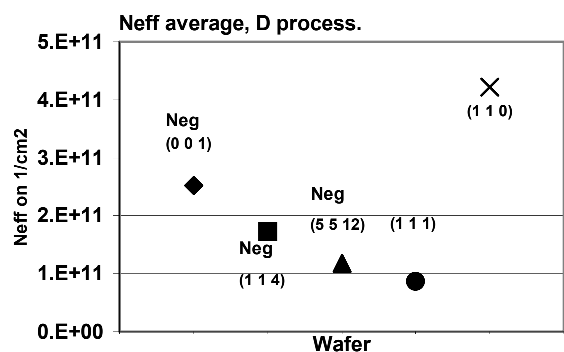

Figure 4. Effective charge density obtained in **D** process. The label **Neg** indicates a negative Q_{eff}.